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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,255	03/21/2001	Shunpei Yamazaki	07977-107002	5578

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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01/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/814,255	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20,28-31,33-38,40-45,47-53,55 and 56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20,28-31,33-38,40-45,47-53,55 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/1/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 41-45, 47-53 and 55-56 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for a part of the first layer is located over the interlayer insulating film, wherein the side recess is filled with the first layer, as recited in claims 41 and 49. Although figure 3C and supporting figure 13 describe the second side recess (of the gate electrode) is filled with the third layer wherein a part of the third layer is located over the interlayer insulating film, figure 3C depicts the first layer (the bottom alloy) filling the side recess (of the source region) as being a separate and distinct layer from layer 320 which is located over the interlayer insulating film.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20, 28, 31, 34-35, 38, 41-42, 45, 47, 49-50, 53 and 55 are rejected under 35 U.S.C. 102(b) as anticipated by Kudoh (5,159,416).

Regarding claims 20, 34, 41 and 49, Kudoh teaches in figure 9 and related text a semiconductor device having a thin film transistor the thin film transistor comprising:

a semiconductor layer 12 on an insulating surface 11, wherein the semiconductor laver has a side recess (the area where layer 15 is located);

a gate electrode 14 adjacent to the semiconductor layer with a gate insulating film 13 interposed there-between, wherein the gate electrode has a second side recess and a wiring 17 in contact with the gate electrode; and

an interlayer insulating film 98 comprising silicon oxide over at least the gate electrode; and

a source electrode 15, 97 over the interlayer insulating film, wherein the source electrode is in contact with the semiconductor layer through a contact hole opened in the interlayer insulating film 98, wherein the source electrode contains a first layer 15 and a second layer 97;

wherein a part of the first layer, a part of the second layer, a part of the third layer and a part of the fourth layer are located over the interlayer insulating film,

wherein the wiring contains a third layer 17 and the fourth layer (the wiring connected to layer 125, see figures 11A and 11B),

wherein the side recess is filled with the first layer 15, and

wherein the second side recess is filled with the third layer, and

wherein the first layer 15 is in contact with the gate insulating film 13.

Please note that a part of the first layer is located over the interlayer insulating film, because a part of the first layer is located at higher elevation (higher is synonymous to "on", "over" and "above") than the interlayer insulating film. The broad recitation of the claims does not require that a part of the first layer is located directly over the interlayer insulating film.

Regarding claims 28, 35, 42, 47, 50 and 55, Kudoh teaches in figure 9 and related text a semiconductor layer contains crystalline silicon, and a silicon oxide interlayer insulating film.

Regarding claims 31, 38, 45 and 53, Kudoh teaches a second layer contains aluminum.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 29, 36, 43 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh in view of Aratani et al. (5,854,139).

Kudoh teaches substantially the entire claimed structure, as applied to claims 20, 34, 41 and 49 above, except a first layer contains at least one selected from the group consisting of germanium, tin, gallium, zinc, lead, indium, and antimony.

Aratani et al. teach a source electrode comprising indium silicide (column 8, line 64 to column 9, line 1).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Kudoh's silicide layer of indium silicide, in order to improve the characteristics of the device. Note that substitution of materials is not patentable even when the substitution is new and useful. Safetran Systems Corp. v. Federal Sign & Signal Corp. (DC NIII, 1981) 215 USPQ 979.

Claims 33, 40, 48 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 33, 40, 48 and 56, Kudoh teaches substantially the entire claimed structure, as applied to claims 20, 34, 41 and 49 above, except using the device as an active matrix type EL display device.

AAPA teaches using thin film device as an active matrix type EL display device.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Kudoh's device as an active matrix type EL display device, in order to use the device in an application which requires an active matrix type EL display device.

Claims 30, 37, 44 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudoh in view of Tanaka et al. (5,798,744).

Kudoh teaches substantially the entire claimed structure, as applied to claims 20, 34, 41 and 49 above, except a first layer is an alloy of aluminum and germanium.

Tanaka et al. teach a first layer can be silicide or germanium compound (column 9, lines 56-61).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first layer comprises germanium compound instead of silicide in Kudoh's device, in order to improve the device characteristics.

Note that forming a first layer comprises germanium, as taught by Tanaka et al., and a second layer of aluminum, as taught by Kudoh mean that the first layer would comprise aluminum-germanium, because the aluminum would react with the germanium.

Note that substitution of materials is not patentable even when the substitution is new and useful. Safetran Systems Corp. v. Federal Sign & Signal Corp. (DC NIII, 1981) 215 USPQ 979.

Response to Arguments

Applicant argues that Kudoh does not teach a semiconductor laver having a side recess, because the area where layer 15 is located is not a "side" recess, as claimed.

It is unclear to the examiner why the recess where layer 15 is located cannot be called a side recess. The examiner respectfully requests clarification.

Applicant argues that Kudoh does not teach a first layer located over the interlayer insulating film, because layer 15 of Kudoh is not located over the interlayer insulating film.

A part of the first layer is located over the interlayer insulating film, because a part of the first layer is located at higher elevation (higher is synonymous to "on", "over" and "above") than the interlayer insulating film. The broad recitation of the claims does not require that a part of the first layer is located directly over the interlayer insulating film.

Applicant requests clarification as to which layer is the fourth layer.

Figures 11A and 11B depict plurality of wiring connections, connecting layer 125 to various elements of the circuit. Any of these wiring connections is the fourth layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
1/4/08

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